Laser Diode Adaptive Power Controller

PRELIMINARY

FEATURES

- **Integrated Bias Current Monitor**
  - **Monitors & Measures Laser Temperature Directly**
  - **Eliminates Need for External Thermistor & Thermal Coupling Issues**
  - **Alarm Output on Over-temperature Condition**
- **Adaptive Modulation Control (AMC)**
  - **Adjusts Modulation Current as a Function of the Laser Temperature**
  - **8 × 8 Programmable Compensation Table**
  - **256 Independent Compensation Values**
  - **Integrated 8-Bit Modulation Control DAC**
- **Flexible Biasing Architecture**
  - **Bias Control and Modulation Control: 0 to 10mA / 0 to 100 mA Source, 0 to 100mA Sink**
- **Automatic Power Control (APC) with Integrated 10-Bit Programmable Offset**
  - **Automatic Initial Bias Optimization**
- **Electronic Calibration Through 2-wire Interface**
- **3V or 5V Operation**

DESCRIPTION

The SML2108 is an adaptive power controller for laser diodes. It is the industry's first integrated device that can directly monitor and measure a laser diode's temperature, and provide a variable modulation current. The SML2108's integrated active feedback loop is used to calibrate and control the mean and modulation power of high speed, high power laser diodes.

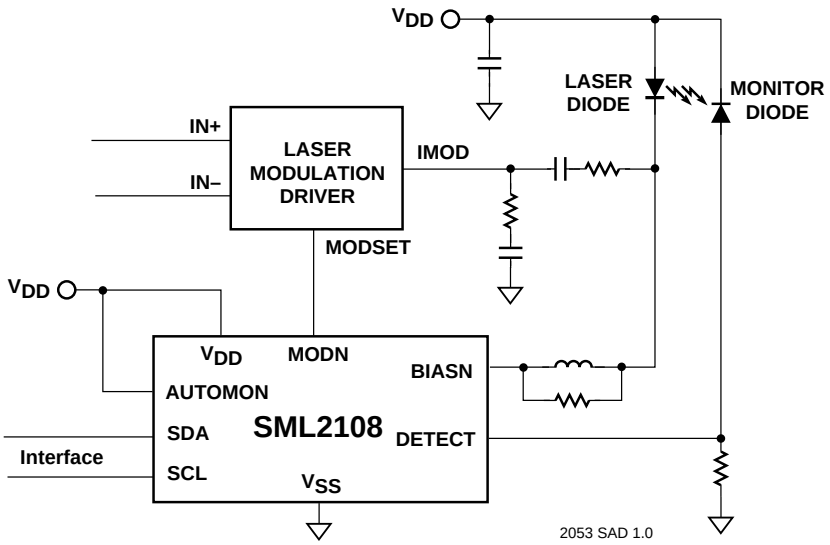
Inherent manufacturing tolerances introduce variations of performance in laser diodes. These variations, combined with parametric changes over the laser's extreme temperature range and laser ageing, call for an efficient temperature compensation scheme. Using an internal digital control loop and a programmable nonvolatile compensation lookup table, the SML2108 provides the most optimum adaptive power control with a minimum number of external components.

The SML2108 removes the need for any manual calibration of the laser control circuit, which is currently the industry standard practice. All calibration values are programmed through the 2-wire communication interface, which can be controlled by most production ATE equipment.

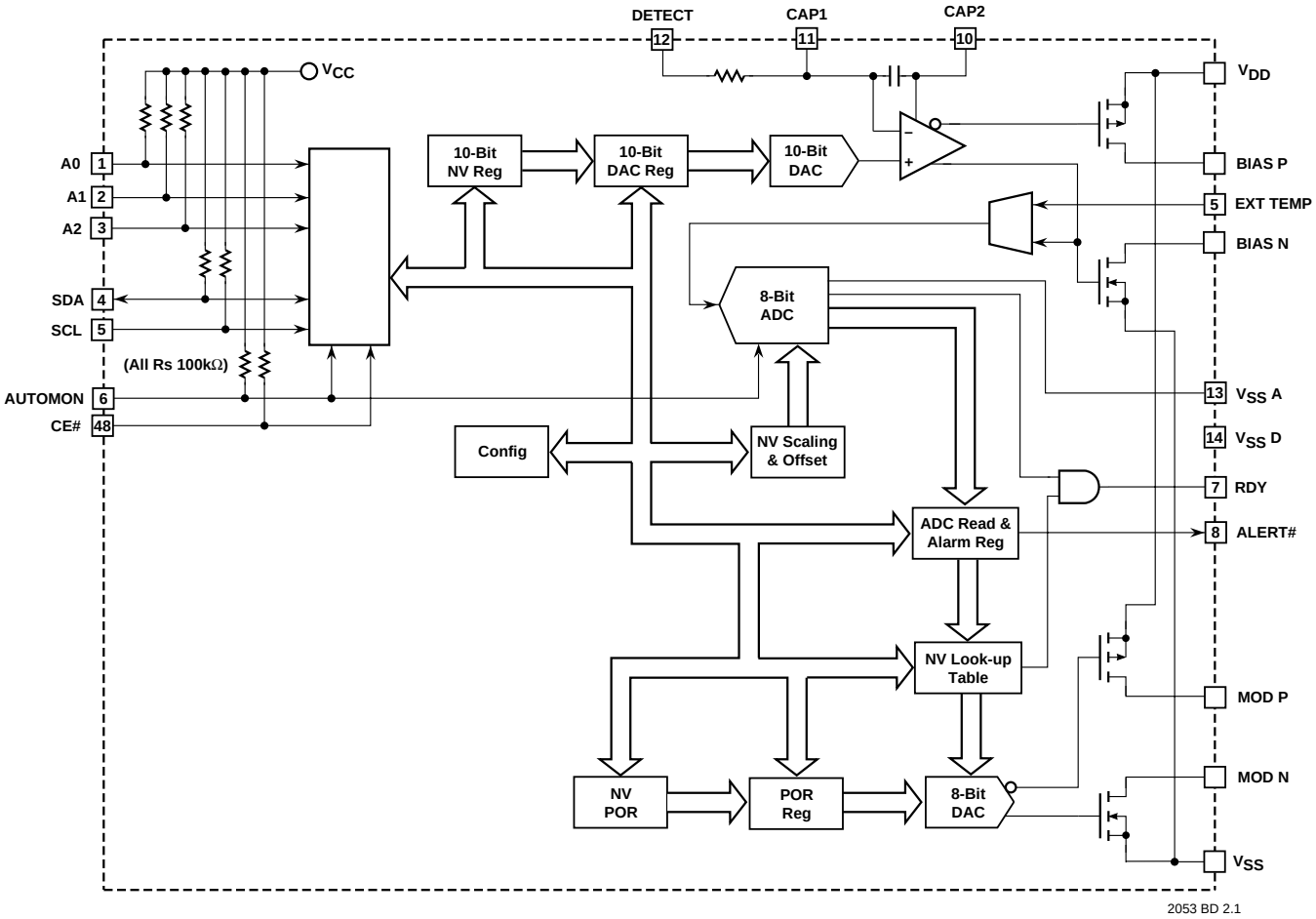
Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

The SML2108 is available in 48 lead TQFP.

SIMPLIFIED APPLICATION DIAGRAM

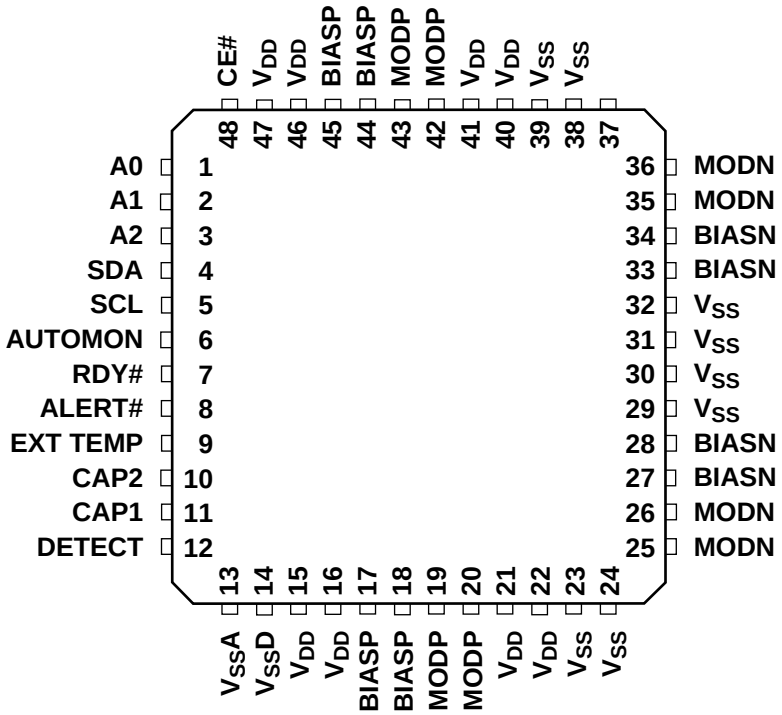


FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

48-Pin TQFP



2053 PCon 2.0

PIN DESCRIPTIONS

DETECT (12)

This is the analog input from the laser monitor photodiode for the integrator circuit. There is an on-board resistance of 2MΩ between the DETECT input and CAP1 pin.

CAP1 and CAP2 (11 & 10)

Capacitor inputs for an external capacitor in the feedback loop of the Mean Power Control Integrator. There is an on-board capacitance of 500pF.

AUTOMON (6)

Active high input used to enable the internal auto-monitor function, which provides automatic adjustments to the modulation output currents (MODP and MODN) based on the internal A/D output and the values stored in the nonvolatile lookup table. This pin has an internal 100kΩ pullup.

ALERT# (8)

Active low, open-drain output. This pin is driven low whenever the bias current increases beyond a predefined nonvolatile threshold. This can be used to predict laser failure.

SDA, SCL (4 & 5)

Data and Clock lines, respectively, whose function and use are based on the industry standard I^2C interface. Lookup table values, configuration data, and D/A and A/D registers may all be accessed via these two pins of the SML2108. These pins have internal 100kΩ pullups.

A0, A1, A2 (1, 2, & 3)

Address Pins for the interface provided to allow multiple devices on a single bus. These pins have internal 100kΩ pullups.

RDY# (7)

Active low, open-drain output. This pin is driven low whenever the internal A/D is performing a conversion, or while the on-board EEPROM is being programmed.

EXT TEMP (9)

Temperature input (or no connection). This pin can be programmed as an input to the ADC and can interface a temperature sensor. The EXT TEMP pin is multiplexed with the bias current to provide a means of configuring the input to the ADC. When EXT TEMP is programmed as the

input to the ADC using bit 5 of Register 1, the converted value of the current entering this pin is used as the address of the EEPROM lookup table. In this configuration the modulation current can be controlled by temperature rather than the bias current. Refer to the application example on using the EXT TEMP pin. If this option is not used the pin should be left floating.

V_{SS}A, V_{SS}D (13 & 14)

Analog and digital low-side supplies for on-board circuitry. Must be at same potential as all other VSS pins.

V_{DD} (15, 16, 21, 22, 39, 40, 45, 46, & 47)

High-side supply for the Bias and Modulation currents and power supply input for the chip.

CE# (48)

The chip enable input is active low and provides an additional method of enabling the serial interface. The state of this pin has no effect on the auto-monitor function. This pin has an internal 100kΩ pullup.

BIASP (17, 18, 43, & 44)

High-side mean bias control current. Current source output range is programmable, with the optional ranges of 0 to 100mA or 0 to 10mA.

BIASN (27, 28, 33, & 34)

Low-side mean bias control current. Current sink input range is 0 to 100mA.

MODP (19, 20, 41, &42)

High-side modulation control current. Current source output range is programmable, with optional ranges of 0 to 100mA or 0 to 10mA.

MODN (25, 26, 35, &36)

Low-side modulation control current. Current sink input range is 0 to 100mA.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10 secs) ..... 300 °C

***COMMENT**

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

ELECTRICAL TABLES

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Typical ADC Performance						
S/N	Signal to Noise ratio	T_A = 25ºC	70			dB
THD	Total harmonic distortion		–80			dB
	Peak harmonic intermodulation distortion	2nd Order	–80			dB
		3rd Order	–80			dB
DC Accuracy						
	Resolution			8		Bits
	Reolution for which no missing codes are guaranteed		8			Bits
	Relative accuracy			±½		LSB
DNL				±1		LSB
	Positive full scale error			±2		LSB
	Unipolar offset error	V_{SS} = 5V		±2		LSB
		V_{SS} = 2.7V to 3.6V		±2		LSB

2053 Elect Table A

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	Maximum bias and modulation current	3		5.5	V
I_D	Supply current	Bias and modulation current outputs open		2		mA
I_{LO}	Input leakage current	V_{IN} = 0V to V_{DD}			1	µA
I_{LI}	Output leakage current	V_{OUT} = 0V to V_{DD}			10	µA
V_{OL}	Output low voltage	I_{OL} = 2mA			0.4	V
V_{OH}	Output high voltage	V_{DD} = 5V, I_{OL} = –400µA	2.4			V
		V_{DD} < 4.5V, I_{OL} = –100µA	V_{DD} – 0.2			V
V_{IL}	Input low voltage		–0.1		$0.3 \times V_{DD}$	V
V_{IH}	Input high voltage		$0.7 \times V_{DD}$		0.5	V
f_{INT}	Integrator loop frequency				1	kHz
t_{PUS}	Power up stabilization time	Integrator time constant is less than 10ms			10	ms
Analog Inputs						
DETECT	DETECT input to ADC		0		1.5	V
$I_{EXT\ TEMP}$	Full scale current input			390.6		µA
Analog Outputs						
I_{MODN}	N-channel modulation current		0		–100	mA
I_{MODP}	P-channel modulation current		0		100	mA
I_{BIASN}	N-channel bias current		0		–100	mA
I_{BIASP}	P-channel bias current		0		100	mA
V_{DAC}	10-Bit DAC output		0		1.5	V
Digital Outputs						
ALERT	ALERT output	Open drain ALERT output is active			5	mA

2053 Elect Table B

DEVICE OPERATION

General Description

The SML2108 is an adaptive power controller for laser diodes with an active feedback loop used to calibrate and control the mean and modulation power of high speed, high power laser diodes. Inherent manufacturing tolerances introduce variations of performance in laser diodes. These variations, combined with parametric changes over the laser's extreme temperature range and laser ageing, call for an efficient compensation solution. The SML2108, with a minimum number of external components, is designed to compensate for these tolerances using a digital control loop and a programmable nonvolatile calibration lookup table.

Figure 1 illustrates the usefulness of the SML2108. The figure shows the output light power of a laser diode versus its operating current. Depicted in the graph are typical laser diode characteristics at two different temperatures. At the first temperature (T_1), the laser requires an average bias current of $IBIAS_1$. The modulation current needed to switch the laser between its on and off state is labeled $IMOD_1$. The ratio of light power of its on state divided by the light power of its off state is referred to as the extinction ratio. Ideally the laser will maintain a constant extinction ratio over its entire operating temperature range, as the receiver module is calibrated to this level. Running the laser driver at a higher extinction ratio indicates that power is being wasted, whereas operating at a lower extinction ratio indicates that data may possibly be lost.

When the laser is operated at a second temperature (T_2) the required bias current is shown as $IBIAS_2$. To maintain a constant extinction ratio as in the T_1 curve the laser requires a modulation of $IMOD_2$. The SML2108 is the industry's first integrated device capable of providing a variable modulation current based on a function of either the bias current or an external temperature. This ability to be able to compensate the modulation output current enables the system designer to optimize the extinction ratio of the laser driver module.

The SML2108 has been specified to remove the need for any manual calibration of the laser control circuit. All calibration values are programmed through an industry standard 2-wire communication interface, whose protocol and function can be controlled by most production ATE equipment.

Bias Current — Mean Power Control

The SML2108 bias current outputs (BIASP and BIASN) establish the average power being delivered to an external laser diode. The output of the laser diode is separately monitored using a local back-face diode, the output of which is tied to the DETECT pin of the SML2108. When coupled with the on-board integrator this feedback loop becomes the mean power control for the laser diode. The output block of the mean power control is shown in Figure 2.

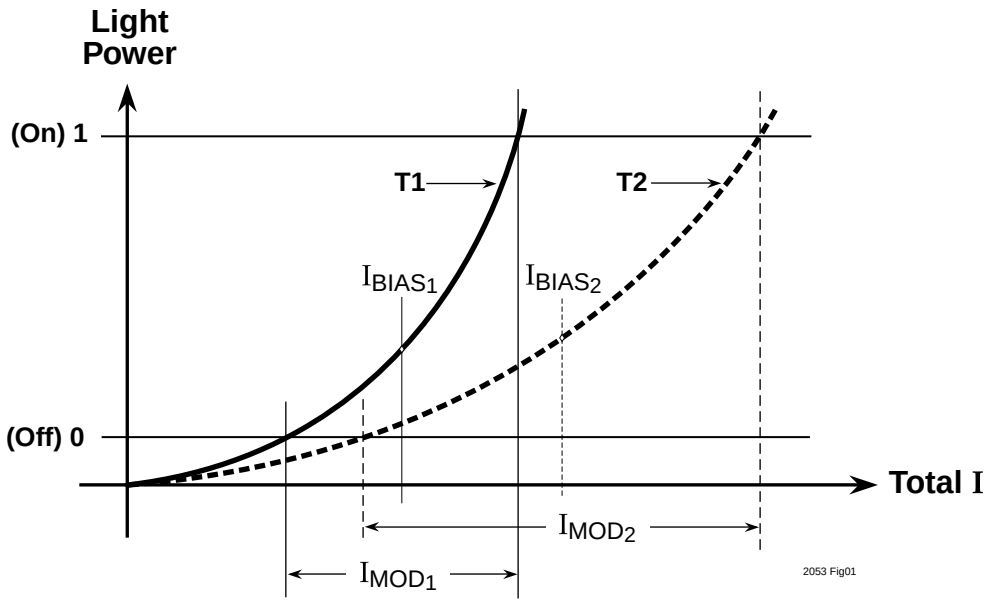


Figure 1. Laser Current Increase Caused by Temperature Increase, Constant Light Power Out

The built-in integration time constant is nominally 1ms. This is accomplished by using an internal 2MΩ resistor and 500pF capacitor. The time constant can be modified by adding external capacitance between the CAP1 and CAP2 terminals, and/or by adding external resistance between the DETECT and CAP1 terminals. For stability reasons it is not recommended that the time constant be decreased to less than 100us.

The output of an internal 10-Bit DAC biases the positive terminal of the integrating amplifier. This DAC provides an analog reference to the integrator which is useful for initial calibration of the laser module. The full-scale value of the DAC output is 1.5V.

10-Bit Bias Control D/A

The 10-Bit D/A determines the reference voltage of the non-inverting terminal of the integrating amplifier in the mean power control loop. Associated with this DAC are a 10-Bit volatile register and a 10-Bit nonvolatile (NV) register. The content of the volatile register determines the DAC output voltage. The DAC output voltage is given by the following relation:

$$OV = \frac{X}{1024} \times 1.5V$$

where X = the decimal equivalent of the 10-Bit data stored in the volatile register. Note that the DAC output voltage is not directly accessible external to the chip. However, when the SML2108 is placed in a typical application circuit, the mean power control feedback loop forces the voltage at the DETECT pin to be the same as the DAC output. On device power-up the volatile register may be loaded with all zeroes, or it may be loaded from the contents of the 10-Bit nonvolatile register.

Access to the 10-Bit volatile register is obtained via the 2-wire interface at slave address 1001_{BIN}, word address 0. Refer to Figures 9, 10, 12, and 13 for details on programming and reading data from the 10-Bit register. When writing to the volatile register the new DAC output will become valid immediately at the end of the write command. Reading the volatile register has no effect on the DAC output. Reading or writing the volatile register has no effect on the contents of the nonvolatile register.

The 10-Bit NV register can only be accessed indirectly through the volatile register. The command sequence to communicate with the NV register is the same as that of the volatile register, except word address 2 is used instead of 0. When reading the NV register, the data is first transferred into the volatile register where it may be accessed by the serial interface. Note that upon this transfer the DAC output will change immediately to reflect the new data. Similarly, when writing to the NV register,

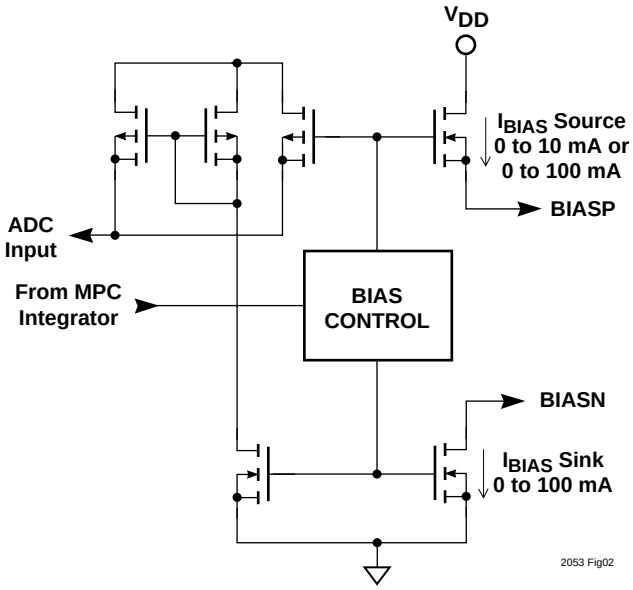


Figure 2. Output Block 1: Mean Power Control

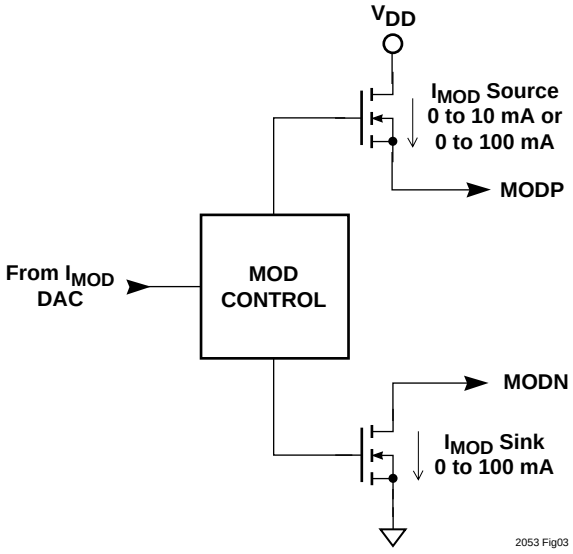


Figure 3. Output Block 2: I_{MOD}

the data is first placed in the volatile register. At the conclusion of the write command an internal nonvolatile write sequence initiates the storage of the volatile contents into the NV register.

Note that when modifying the 10-Bit DAC output, the mean power control loop will become temporarily disrupted. It may be several milliseconds before the bias current has settled to its steady state value. Until then its value will be undefined.

Modulation Current — Auto-Monitor Control

The laser bias current, which relates directly to laser temperature, can be monitored using an on-board, current-sensing A/D converter. In the auto-monitor mode the 8-Bit output of the converter is used as an address to the EEPROM lookup table. The subsequent 8-Bit data output from the lookup table becomes the input for the compensation DAC. The 8-Bit compensation DAC output is a current in the range of 0 to 100mA and is used to control the modulation current MODP and MODN. The output block of the modulation current control is shown in Figure 3.

The lookup table provides an arbitrary mapping from bias current to modulation current. The input range to the ADC may be scaled and/or offset to provide maximum resolution within the appropriate conversion space. The sample interval is programmable from 10µs to 1s. Refer to the ADC section for further details about configuring the A/D. The interface is used to program the configuration registers as well as lookup table values.

Lookup Table

A 2k-Bit (256 x 8) memory array of on-board EEPROM comprises the internal lookup table. This array is accessed via the 2-wire serial interface using a slave address of 1010_{BIN}. (Note: 1010_{BIN} is the default, however this may be set to 1110_{BIN}, depending upon the contents of Configuration Register 2.) Refer to the Bus Interface section for details on programming and reading data from the device.

In the auto-monitor mode the content of the array represents the transfer function between the A/D output and the final value of modulation current. Using a lookup table to implement this function allows arbitrary functions, and even nonlinear relations, to be easily realized. Also, the use of a lookup table allows each device to be customized to normalize overall module operation.

Although the memory may normally be read and written as a standard memory, a security feature exists in the configuration settings that will prevent any external access to the array. Additionally, if the auto-monitor feature is not used, then the modulation output current may be programmed to a fixed value, and the array may be used as a standard memory to store device settings, board identification values, production dates, *etc.*

8-Bit Current Output D/A

The 8-Bit D/A defines the modulation output current. Associated with this DAC are an 8-Bit volatile register and an 8-Bit nonvolatile (NV) register. The content of the volatile register determines the DAC output current. The DAC output current is given by the following relation:

$$OC = \frac{X}{256} \times 100mA$$

where X = the 8-Bit data stored in the volatile register. On device power-up the volatile register may be loaded with all zeroes or it may be loaded from the contents of the 8-Bit nonvolatile register.

Access to the 8-Bit volatile register is obtained via the 2-wire interface at slave address 1001_{BIN}, word address 4. Refer to Figures 8 and 11 for details on programming and reading data from the 8-Bit register. When writing to the volatile register, the new DAC output will become valid immediately at the end of the write command. Reading the volatile register has no effect on the DAC output. Reading or writing the volatile register has no effect on the contents of the nonvolatile register.

The 8-Bit NV register can only be accessed indirectly through the volatile register. The command sequence to communicate with the NV register is the same as that of the volatile register, except word address 6 is used instead of 4. When reading the NV register the data is first transferred into the volatile register where it may be accessed by the serial interface. Note that upon this transfer the DAC output will change immediately to reflect the new data. Similarly, when writing to the NV register, the data is first placed in the volatile register. At the conclusion of the write command, an internal nonvolatile write sequence initiates the storage of the volatile contents into the NV register.

ADC SCALING AND OFFSET

The ADC can be customized to monitor a particular range of bias current by programming Register 0. Bits 3 and 2 control the scaling of the ADC while bits 1 and 0 control the ADC offset. The four graphs (Figures 4, 5, 6, & 7) illustrate the ADC scale values, according to the two bit code. In each Graph the curves are differentiated by the ADC offset values. Note: if using I_{BIASP} with the maximum current option set to 10 mA, divide the x-axis value by 10 (*i.e.*, 75 = 7.5, *etc.*).

These combinations of scales and offsets allow the resolution to be maximized over a given range of current. For example, if the bias current is known to be in the range of 30mA to 70mA the choice would be the Half scale graph (code 10_{BIN}) and the ¼ offset curve (code 01_{BIN}) to maximize the resolution of the ADC.

Note that these graphs assume a full scale bias current of 100mA. When the ADC is configured to receive input from the EXT TEMP pin full scale current becomes 390.6µA, which limits the internal 1/256 scale factor between bias current and the ADC input current.

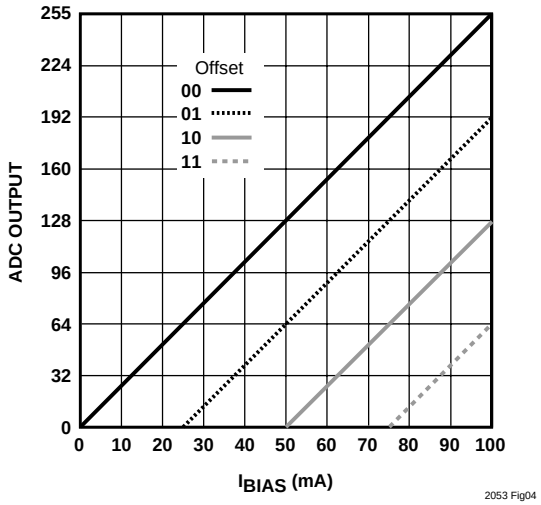


Figure 4. Full Scale (code 11_{BIN}) with Offset

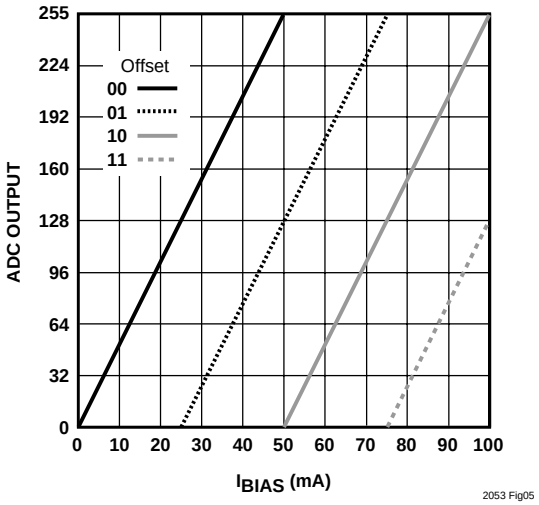


Figure 5. Half Scale (code 10_{BIN}) with Offset

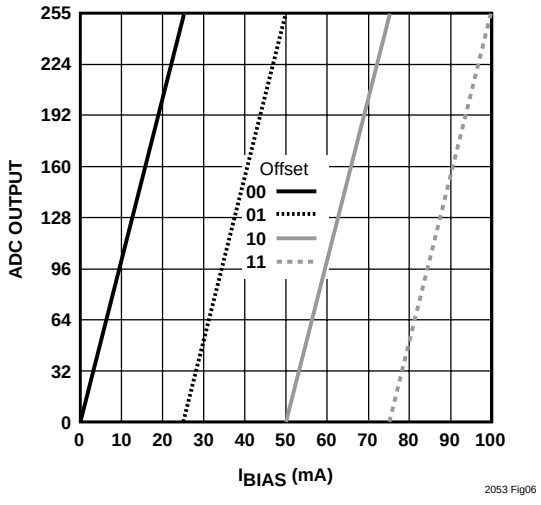


Figure 6. Quarter Scale (code 01_{BIN}) with Offset

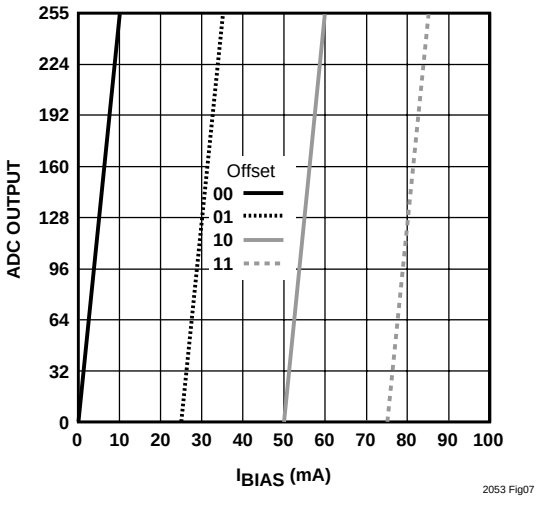


Figure 7. Tenth Scale (code 00_{BIN}) with Offset

REGISTERS

REGISTER BIT MAPS

The SML2108 has three user programmable, nonvolatile configuration registers.

Register 0

This register is used to configure the 8-Bit ADC that monitors the bias current. Bit 7 enables the ADC alert to be latched, which will hold the ALERT pin low until the alert is reset. Bits 6, 5, and 4 are used to set the sample interval of the ADC. The input to the ADC can be scaled and offset to provide maximum resolution over the bias current. Bits 3 and 2 are used to set the full scale range of the ADC, while bits 1 and 0 are used to set the ADC offset. See the Table.

Register 1

This register controls multiple functions. Bit 7 disables the alert during a manual analog-to-digital conversion of the bias current. Bit 6 selects the action that will reset an alert from the ADC. When this bit is set to a 0 any device read or write will reset the alert. When set to a 1 the alert will be reset by a low AUTOMON signal. Bit 5 is used to toggle the source of the ADC input between the I_{BIAS} current and the EXT TEMP signal. Bit 2 initializes the input of the 10 bit DAC to either zero or a stored value from a nonvolatile register when the device is powered up. Bit 1 initializes the input of the 8 bit DAC to either zero or a stored value from a nonvolatile register when the device is powered up. Bit 0 sets the maximum P-channel bias current (I_{BIASP}) and modulation current (I_{MODP}) to either 10mA or 100mA.

Register 2

This register controls several functions related to the bus interface. Bits 7 and 6 control the read and write access to the configuration registers. It is imperative that register 2 be programmed properly to prevent an inadvertent lockout. Bit 5 determines whether the memory array is available or locked. Bit 4 selects the device type address for accessing the memory array, while bit 3 determines whether the device must receive a bus address that corresponds to the biasing of the address pins. Bit 2 is used to enable an alert condition on the ADC to shut down the bias current. Bits 1 & 0 are unused.

7	6	5	4	3	2	1	0	Function
ADC Alert	**ADC Sample Interval**			**ADC Range**		**ADC Offset**		
0	x	x	x	x	x	x	x	Alert not latched
1								Alert latched
x	**0**	**0**	**0**					5µs sample interval
	0	**0**	**1**					20µs " "
	0	**1**	**0**					160µs " "
	0	**1**	**1**					1.28ms " "
	1	**0**	**0**					6.25ms " "
	1	**0**	**1**					25ms " "
	1	**1**	**0**					200ms " "
	1	**1**	**1**					1.6s " "
	x	x	x	**0**	**0**			1/10 full scale bias current
				0	**1**			1/4 full scale bias current
				1	**0**			1/2 full scale bias current
				1	**1**			Full scale bias current
				x	x	**0**	**0**	No offset
						0	**1**	1/4 of full scale bias current offset
						1	**0**	1/2 of full scale bias current offset
						1	**1**	3/4 of full scale bias current offset

2053 Reg0 1.0

Register 0

7	6	5	4	3	2	1	0	Function
Alert	**Alert Reset**	**ADC Input**	**Unused**		**10-Bit DAC**	**8-Bit DAC**	**I_{BIASP}**	
0	x	x	x	x	x	x	x	Alert not allowed during manual conversion
1								Alert allowed during manual conversion
x	**0**							Alert reset by Read or Write
	1							Alert reset by Low on AUTOMON pin
	x	**0**						I_{BIASN} or I_{BIASP} current input to ADC
		1						EXT TEMP pin input to ADC
		x			**0**			Input to DAC is zero on power up
					1			Input to DAC is from nonvolatile register on power up
					x	**0**		Input to DAC is zero on power up
						1		Input to DAC is from nonvolatile register on power up
						x	**0**	Max current is 10mA: I_{BIASP} , I_{MODP}
							1	Max current is 100mA: I_{BIASP} , I_{MODP}

2053 Reg1 1.0

Register 1

7	6	5	4	3	2	1	0	Function
Register Access		**Memory Access**	**Device Address**	**Pin Address**	**Alert Action**	**Unused**		
0	**0**	x	x	x	x	x	x	All Registers locked; no Read or Write
0	**1**							Read all Registers; no Write
1	**0**							Write all Registers; no Read
1	**1**							Read and Write all Registers
x	x	**0**						EEPROM available
		1						EEPROM locked
		x	**0**					Device Type Adress is 1010_{BIN}
			1					Device Type Adress is 1110_{BIN}
			x	**0**				Responds to address pin biased address only
				1				Responds to any bus address
				x	**0**			Bias current unaffected by alert condition
					1			Alert condition shuts down bias current

2053 Reg2 1.0

Register 2

BUS INTERFACE

GENERAL DESCRIPTION

The I²C bus is a two-way, two-line serial communication between different integrated circuits. The two lines are: a serial Data line (SDA) and a serial Clock line (SCL). All Summit Microelectronics parts support a 100kHz clock rate, and some support the alternative 400kHz clock. Check the AC Electrical Table for the value of f_{SCL}. The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. Summit parts have a Schmitt input on both lines. See Figure X1 and Table X1 for waveforms and timing on the bus. One bit of Data is transferred during each Clock pulse. The Data must remain stable when the Clock is high.

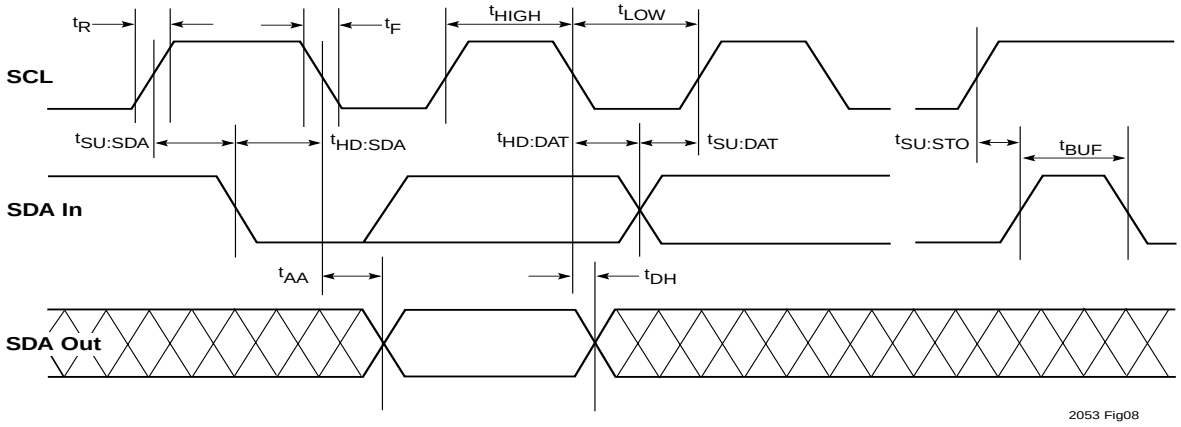


Figure 8. I²C Data Timing

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time			1000	ns
t_F	SCL and SDA fall time			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

2053 Table01 1.0

Table 1. I²C Data Timing

Start and Stop Conditions

Both Data and Clock lines remain high when the bus is not busy. Data transfer between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the Data line while the Clock line is high is defined as a Start condition. A low-to-high transition of the Data line while the Clock line is high is defined as a Stop condition. See Figure 9.

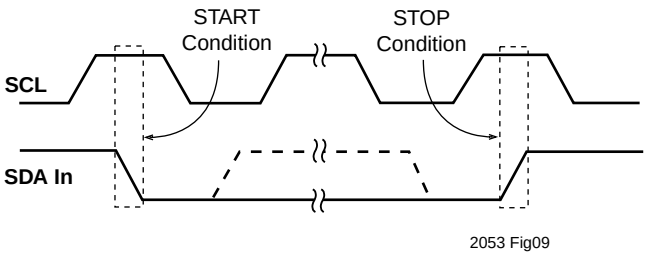


Figure 9. I²C Start and Stop Timing

Protocol

The protocol defines any device that sends data onto the bus as a Transmitter, and any device that receives data as a Receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the Summit Microelectronic devices are slave devices, since they never initiate any data transfers.

Acknowledge

Data is always transferred in 8-Bit bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The Transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the Receiver will pull the SDA line low to Acknowledge that it received the eight bits of data (See Figure 10). The termination of a Master Read sequence is indicated by a non-Acknowledge (NACK), where the Master will leave the Data line high.

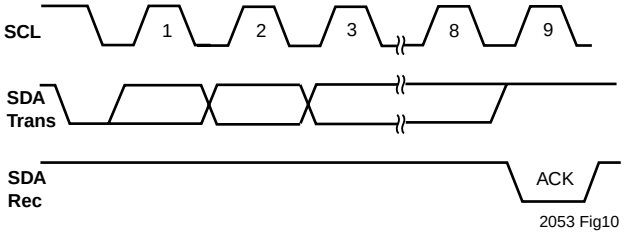


Figure 10. Acknowledge Timing

In the case of a Read from a Summit part, when the last byte has been transferred to the Master, the Master will leave the Data line high for a NACK. This will cause the Summit part to stop sending data, and the Master will issue a Stop on the clock pulse following the NACK.

In the case of a Write to a Summit part the Master will send a Stop on the clock pulse after the last Acknowledge. This will indicate to the Summit part that it should begin its internal non-volatile write cycle.

Read and Write

The first byte from a Master is always made up of a seven bit Slave address and the Read/Write bit. The R/W bit tells the Slave whether the Master is reading Data from the bus or writing Data to the bus (1 = read, 0 = write). The first four of the seven address bits are called the Device Type Identifier (DTI). The DTI for the SML2108 is 1010. The next three bits are not used in the SML2108 (See Figure 11). The SML2108 will issue an Acknowledge after recognizing a Start condition and its DTI.

In the read mode the SML2108 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SML2108 will continue to transmit data. If an Acknowledge is not detected (NACK) the SML2108 will terminate further data transmission. See Figure 12.

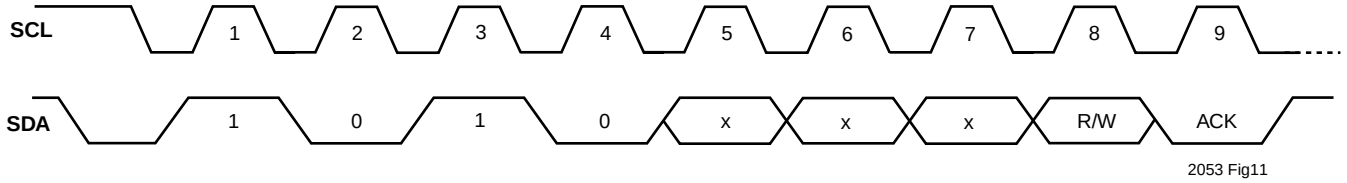


Figure 11. Typical Master Address Byte Transmission

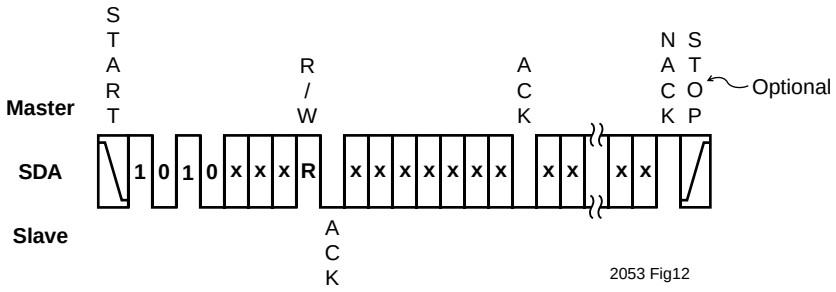


Figure 12. Read

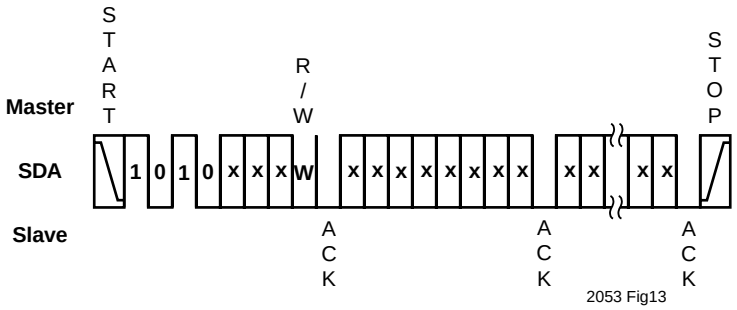


Figure 13. Write

In the write mode the SML2108 receives eight bits of data, then generates an Acknowledge signal. It will continue to generate ACKs until a Stop condition is generated by the Master. See Figure 13.

Random Address Read

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SML2108 to the desired address. After the word address acknowledge is received by the Master, it immediately reissues a start condition followed by another Slave address field with the R/W bit set to Read. The SML2108 will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point, the Master does not acknowledge the transmission, but does generate a Stop condition. The SML2108 discontinues data transmission.

Sequential READ

Sequential Reads can be initiated as either a current address Read or a random access Read. The first word is transmitted as with the other byte read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data. The SML2108 continues to output data for each Acknowledge received. The Master terminates the sequential Read operation by not responding with an Acknowledge, and issues a Stop condition. During a sequential read operation the internal address counter is automatically incremented with each Acknowledge signal. For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will 'roll-over' and the memory will continue to output data.

The protocol for reading and writing to the registers and the lookup table are illustrated in Figures 14 through 24.

TIMING DIAGRAMS

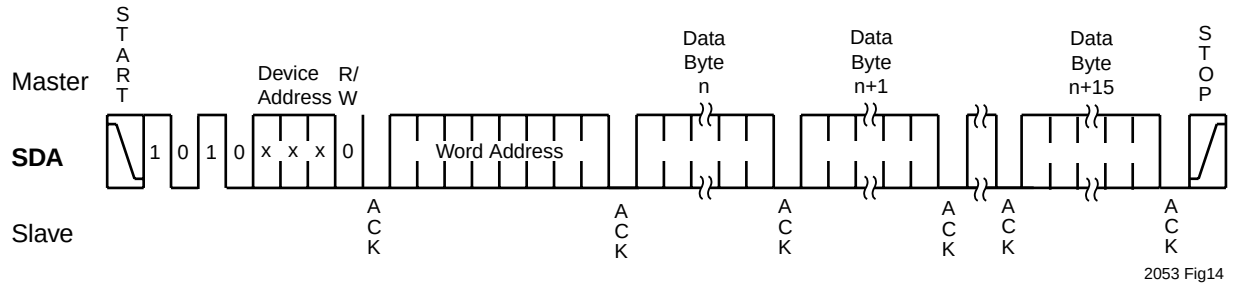


Figure 14. Look-up Table Page/Byte Write

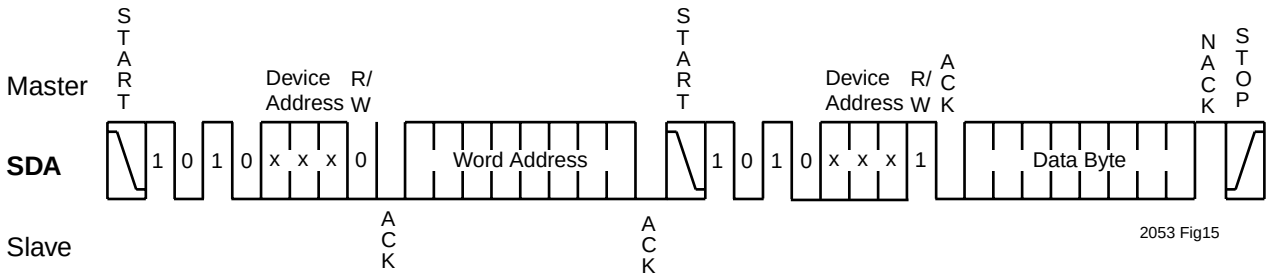


Figure 15. Look-up Table Random Address Read with Dummy Write

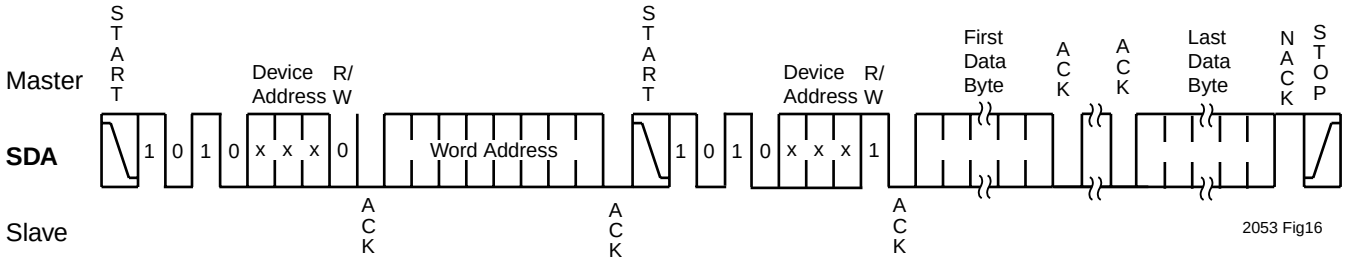


Figure 16. Look-up Table Sequential Read with Dummy Write

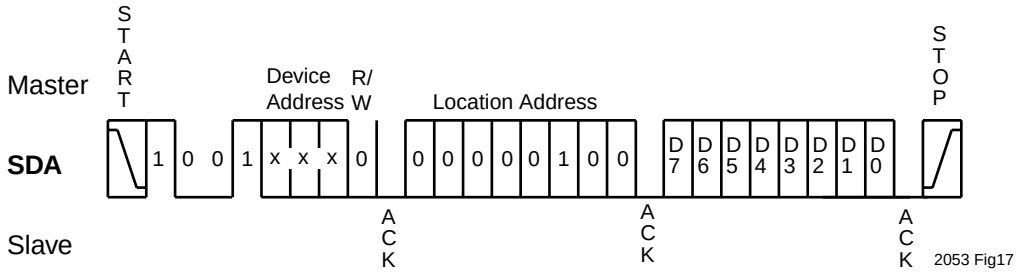


Figure 17. 8-Bit DAC Volatile Register Write

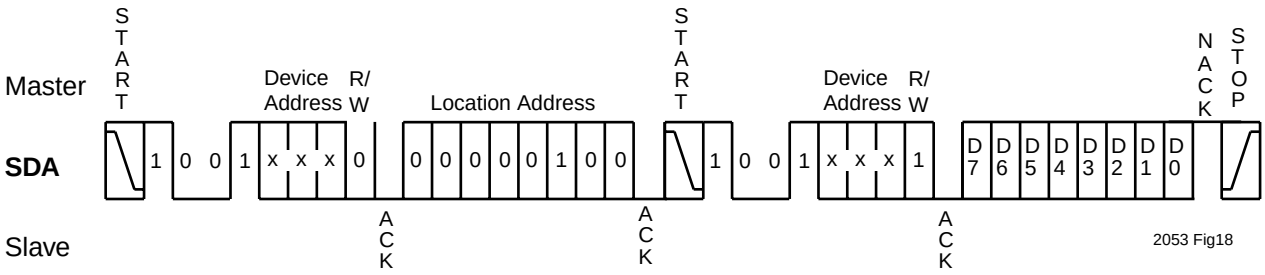


Figure 18. 8-Bit DAC Volatile Register Read with Dummy Write

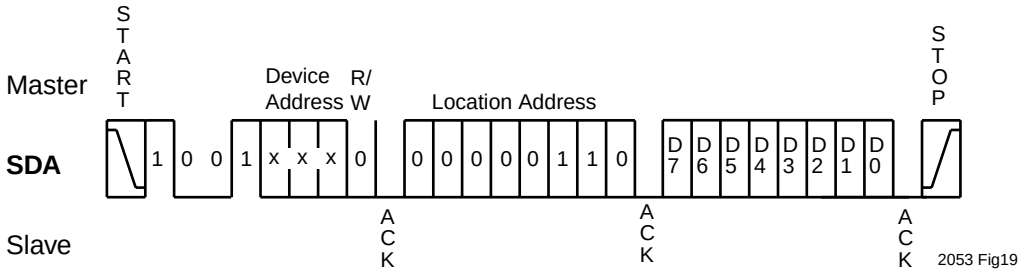


Figure 19. 8-Bit DAC Non-volatile Register Write

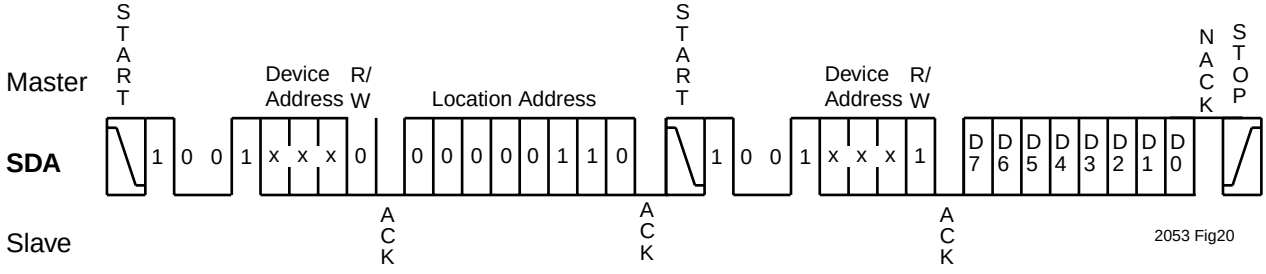


Figure 20. 8-Bit DAC Non-volatile Register Read with Dummy Write

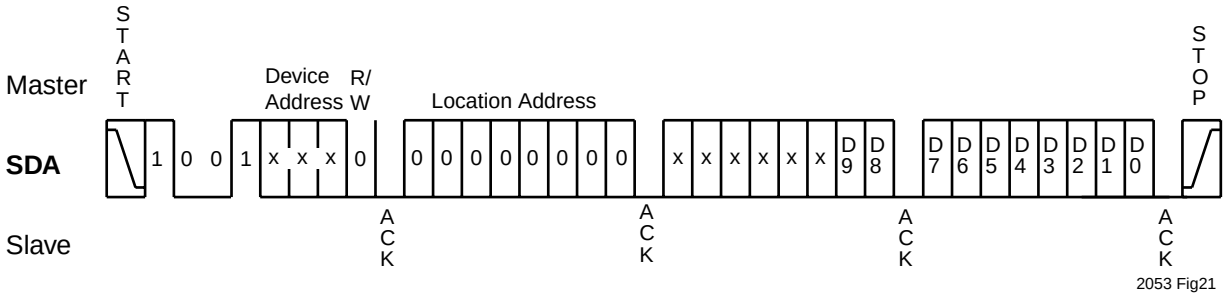


Figure 21. 10-Bit DAC Volatile Register Write

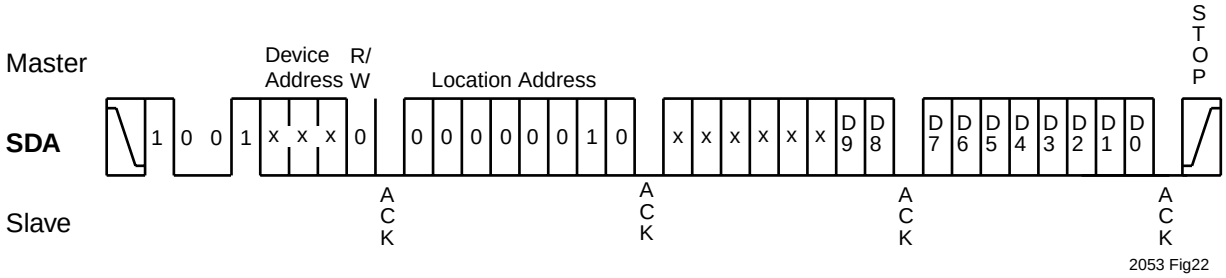


Figure 22. 10-Bit DAC Nonvolatile Register Write

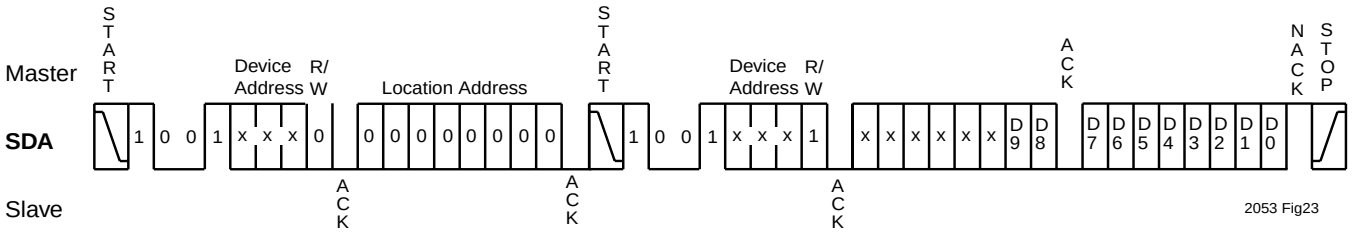


Figure 23. 10-Bit DAC Volatile Register Read with Dummy Write

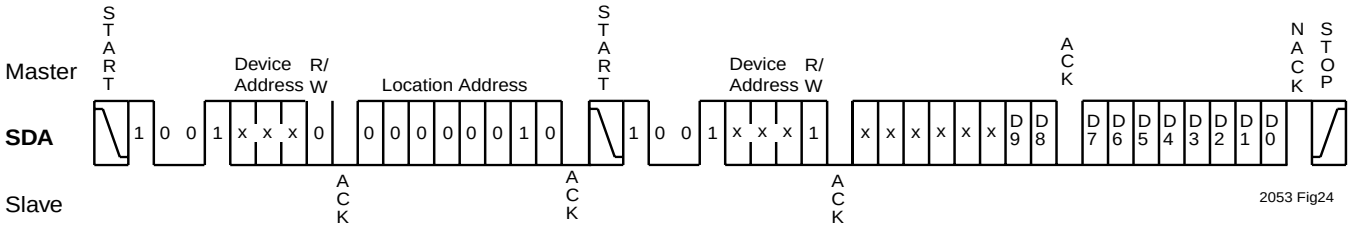


Figure 24. 10-Bit DAC Nonvolatile Register Read with Dummy Write

APPLICATIONS

APPLICATION EXAMPLE USING EXTERNAL TEMPERATURE INPUT

The EXT TEMP pin of the SML2108 allows the input of the internal ADC to be driven from an external device, rather than a mirrored version of the bias current. Figure 25 shows an example using a National Semiconductor LM334 to deliver a current into the SML2108 that is proportional to absolute temperature. The scale and offset features of the ADC input can be used to center this current and maximize the full range of the look-up table.

For this application the current I_{SET} coming out of the LM334 and into the EXT TEMP pin of the SML2108 is given by the following equation:

$$I_{SET} = 227\mu V / {}^{o}K / R_{SET}$$

For example, using a value of 210Ω for R_{SET} yields a current of 295µA at 0ºC and 387µA at 85ºC.

Next select scale and offset values of the ADC input that will optimize the current range of the LM334. Nominal full-scale input current of the ADC is 390.6µA (= 100mA/256). By setting the input offset to ¾ scale (293µA) and the full-scale range to ¼ scale (97.6µA), then the zero scale of the internal ADC becomes 293µA, and the full-scale is 390.6µA. This represents a temperature range of approximately –2ºC to 88ºC using a 210Ω resistor in the configuration shown. (These settings correspond to configuration Register 0, Bits 3 - 0 set to 7_{HEX}.)

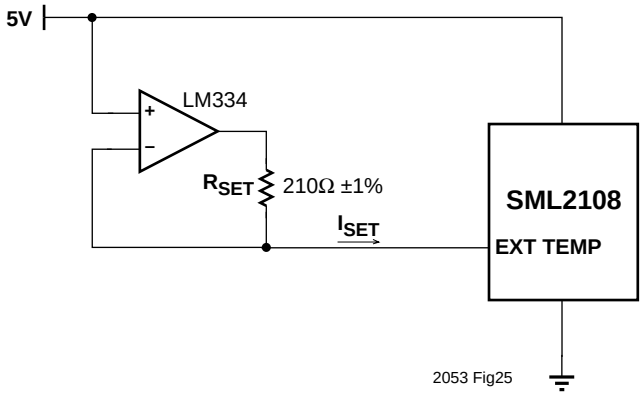
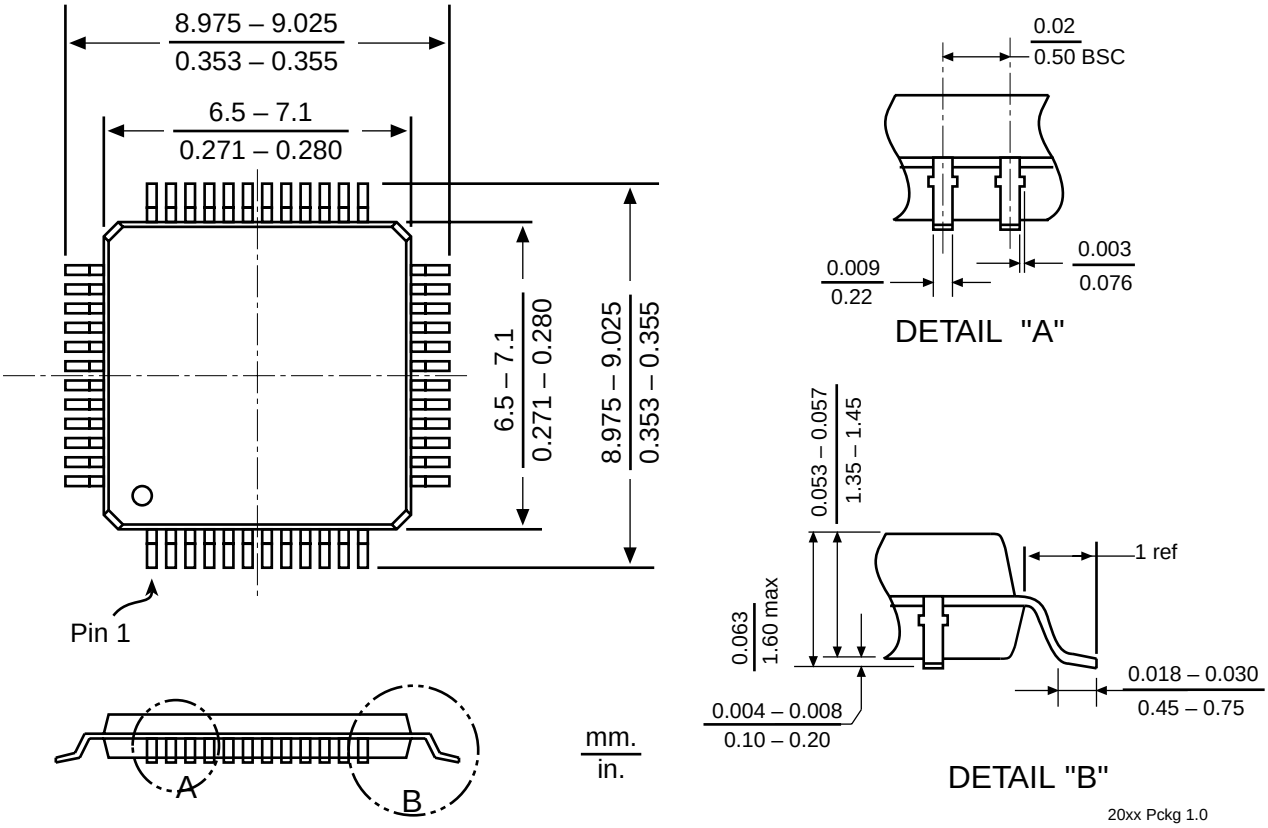


Figure 25. Example of an External Temperature Sensing Device

PACKAGE

48 PIN TQFP PACKAGE



20xx Pckg 1.0

ORDERING INFORMATION

SML2108 F

Base Part Number

Package
F = 48 Pin TQFP

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